REQUESTED AMENDMENT

Please amend the above-identified application as indicated below.

IN THE CLAIMS:

Please replace text of claims 41, 42, 43, 44, 47, 48, and 55 with the following text:

41. A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate;

at least one second well region of the first conductivity type formed in each of the at least two first well regions; and

semiconductor MOSFET elements formed in the at least two first well regions and the at least one second well region,

wherein a memory circuit comprises the semiconductor MOSFET elements.

42. A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate;

a second well region of the first conductivity type formed in each of the at least two first well regions;

integrated circuits which are formed on the at least two first well regions and the second well region, respectively, and which have different functions.

43. A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate;

a second well region of the first conductivity type formed in each of the at least two first well regions;

a third well region of the second conductivity type formed in each of the at least two first well regions; and

integrated circuits formed on each of the at least two first well regions, the second well region and the third well region.

D1

44. The semiconductor integrated circuit device according to claim 42, wherein a second well region of the first conductivity type having a third well region of the second conductivity type formed therein, formed in each of the at least two first well regions; and

one of the integrated circuits formed in the each of the at least two first well regions, the second well region and the third well region.

47. The semiconductor integrated circuit device according to claim 43, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region and the third well region.

D2

48. The semiconductor integrated circuit device according to claim 44, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region and the third well region.

55. The semiconductor integrated circuit device according to claim 43, wherein a back gate bias is supplied to the at least two first well regions, the second well region and the third well region, and an input/output circuit or an interface circuit is formed in the at least two first well regions, the second well region and the third well region.

D3